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PETsys SiPM Readout System

§ 1. Introduction.

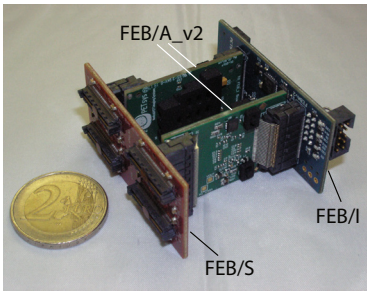

Figure 1. FEM128
The Front-End Module FEM128 has two ASICs and reads 128 SiPM channels. It measures 25.4x53.1x54.0 mm.

The PETsys SiPM readout system is designed for reading a large number of SiPM photo-sensor pixels in applications where a high data rate and excellent time resolution is required. It is based on the TOFPET2 ASIC [1]. This is a low power ASIC with 64 channels optimized for reading SiPMs for Time Of Flight PET applications. The ASIC is the interface between the analog signals from the photo-sensors and the digital readout. Every time one of the 64 channels in the ASIC exceeds the configurable set of thresholds, an event record is created giving the channel number, the time and the charge of the event. The rest of the readout chain only handles digital data. The default version of the ASIC is version 2.c; this version only reads positive signals. Version 2.d allows reading either positive or negative signals. For positive signals it behaves very similar to ASIC2.c

The readout system has four main components: the Front-End Module, the Front-End type D module, the Clock&Trigger module and DAQ board. Together these boards allow assembling a complete and scalable data acquisition system reading tens of thousands of independent SiPM pixels.

§ 2. The PETsys Front-End modules.

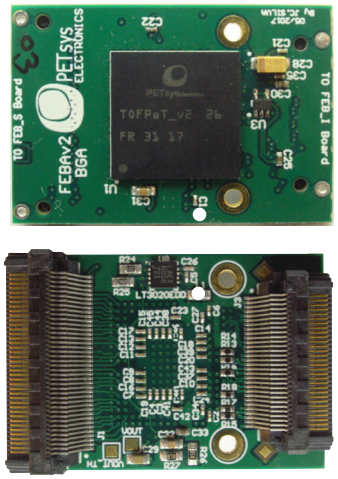

Fig. 2: FEB/A_V2
Top and bottom view. The connector to the right connects to the FEB/S, the connector to the left connects to theFEB/I . The board, including connectors, measures 39x25 mm.

The PETsys Front-End Module is the front-end readout module for reading SiPM arrays, or micro-channel plate photo-detectors. It is the interface between the analog signals of the photo-sensor and the digital readout chain. After the font-end module only digital signals are used. The front-end module may have to be adapted to the particular requirements of the scanner. But we do have 2 “standard”: front end modules: the FEM128 and the FEM256. These are described below.

The Front-End Module version FEM128 (Fig. 1) has 128 channels. It is optimized for systems requiring a high channel data rate. The Front-End Module is made-up from three different boards: FEB/A_V2, FEB/S and FEB/I. This allows for easy customization for different SiPM types and scanner geometries. The FEM128 has two FEB/A_V2 boards (Fig. 2). Each FEB/A board has one PETsys TOFPET2 ASIC with 64 channels. These boards are mounted perpendicular to the SiPM arrays, and this geometry allows to control and stabilize the temperature of the SiPM array. The board also has a temperature sensor near to the ASIC.

The FEB/S board is a purely passive board adapting the SiPM array to the input connector on FEB/A_v2 board .This board will be different for different SiPM array models. The version of the FEB/S board shown on figure 1 has two pairs of connectors that directly take the Hamamatsu S13361-3050AS-08 8x8 MPPC array, or the KETEK 8x8 array PA3325-WB-0808. Each FEB/S measures 53.1 x 25.4 mm and is four-side buttable such as to allow forming a continuously sensitive area with almost no dead space. The FEB/S also has two temperature sensors, each located in the middle between the pair of connectors taking one SiPM array.

Fig. 3: SAMTEC HQCD cable.
A flat coax cable assembly connects the Front-End Module to the PETsys FEB/D board. The standard length is 50 cm, buy this cable can be up to 300cm

The FEB/I allows the FEB/D to communicate with both ASICs and the temperature sensor in the FEM128. It is equipped with a MAX 10 Altera FPGA and adapts the electrical communication protocol from LVCMOS in FEB/D to LVDS in the ASIC and reads the analog temperature sensors. Up to eight FEM128 can be connected to one FEB/D-1k board using a SAMTEC HQDC-030-xx.00-TTL-SBL-1N flat cable (Fig. 3). It is also possible to plug the front-end modules directly into the FEB/D.

The power dissipation of the ASIC is 8.2 mW/channel for the recommended settings. This power dissipation can be reduced to 4 mW/channel by using different settings, but this

[1] Experimental characterization of the TOPET2 ASIC, R. Bugalho et al., JINST_079P_0918

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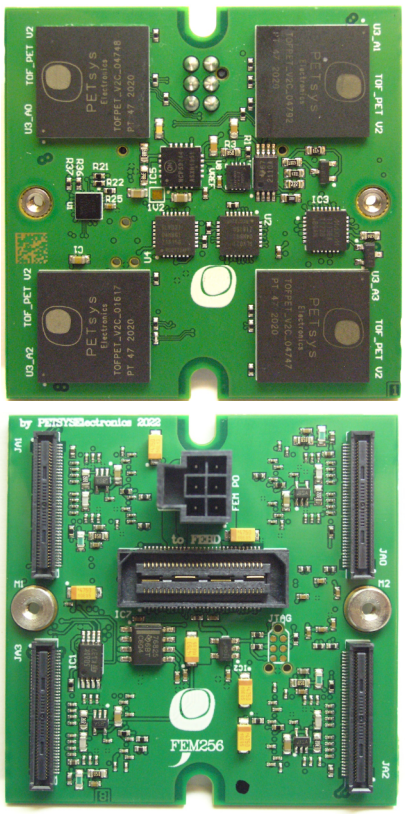

Figure 4. PETsys FEM/256 board.
Figure showing the two sides of the FEM256 board.

results in a slight degradation of the timing performance. The LVDS buffers and LDO voltage regulators of the FEM add 6mW/channel and bring the total power consumption of the FEM at 14.2 mW/channel.

In the FEM128 the data output of the ASIC uses 4 LVDS data lines at up to 800 Mbps per data line. The events are encoded in 80 bits. The maximum event rate between the FEM128 and the FEB/D is about 500 kcps per channel.

The FEM256 is optimized for large systems and lower per channel cost, it allows more compact PET detector modules, and makes the design of the cooling easier.

The board is shown on figure 4. In this front-end board the functionality of the FEB/A and FEB/I of the FEM128 are implemented in one single board. The board is also equipped with a MAX 10 Altera FPGA and adapts the electrical communication protocol from LVCMOS in FEB/D to LVDS in the ASIC and reads the analog temperature sensors. The total power dissipation per channel is again about 14 mW per ASIC channel.

The board measures 50x50 mm^2 and connects to the FEB/D using the same SAMTEC HQC cable (Fig 3). In the FEM256 each ASIC used two LVDS data lines at up to 800 Mbps per data line to output the data. This limits the maximum count rate per channel to 300 kcps.

The FEM256 can connect to the FEB/D-1k, but only four FEM256 can connect to one FEB/D-1k module. The FEM256 is designed to be used with the FEB/D-8k; and up to 16 FEM256 can be connected to one FEB/D-8k. The FEM256 board is connected to a FEB/S board adapted to the FEM256 using flex cables as shown on figure 5.

Figure 5 illustrates how the FEM256 can be integrated with the mechanics and cooling. An aluminum cooling bar is inserted between the FEM256 board(top) and the FEB/S-256 board(bottom) with the SiPM arrays. The SiPM arrays are reflow soldered on the FEB/S-256. The ASICs in the FEM256 are directly in contact with the cooling bar. The cooling bar serves both for the cooling and for positioning the SiPM arrays. The FEB/S-256 measure 52x52 mm^2. Flex cables bring the signals form the SiPM arrays to the ASIC. This figure is only to illustrate the concept. The front end module will probably have to be adapted for the specific scanner design

Figure 5. PETsys FEM/256 detector module.
This figure illustrates how to build a detector module based on the FEM256 board. The cooling solution must be adapted to the particular scanner geometry. .

§ 3. The PETsys Front-End type D module.

The front-end FEB/D module collects event records form the ASICs and send these to the DAQ module in the DAQ computer. It provides power, configuration signals, and clock & synchronization signals to the ASICs, and adjustable bias voltages for the SiPM arrays. Together with the Clock&trigger module it allows system wide coincidence detection in the firmware.

We have two versions of PETsys Front-End type D module. The FEB/D-1k is optimized for medium system with up to maximum 16'384 channels, the FEB/D-8k is optimized for larger systems.

The FEB/D-1k module.

The front end type D module FEB/D-1k is shown on figures 6 and 7. It is composed of a FEB/D motherboard with a Kintex-7 FPGA_XC7K160T, a communication mezzanine, and a bias voltage mezzanine.

Each FEB/D-1k mother board measures 104.5x104.5 mm. Eight front-end modules FEM128 can be connected to one FEB/D-1k board, using either direct board-to-board connectors or using flexible coaxial flat Samtec cables (Fig. 3). The 12V power DC-DC converters and regulators on the FEB/D motherboard provide the low voltages (1.9 V and 3.6 V) for the FEM128.

The upper mezzanine on figure 6 is the communication mezzanine. It has a SFP+ port for data output to the DAQ and for receiving the configuration signals. A second SFP+ port allows the FEB/D to be daisy chained. The SFP+ ports operate at 6.6 Gbit/s allowing a maximum event output rate of 100 Mcps.

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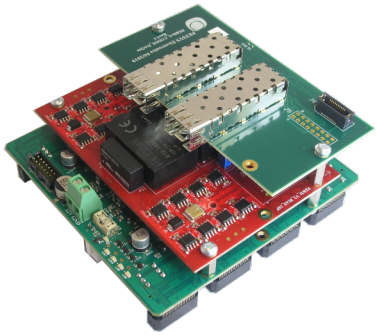

Figure 6: FEB/D-1k module.
Top view of the FEB/D-1k module showing the bias voltage mezzanine (red) and the SFP+ communication mezzanine (green) on top of it..

Synchronous readout of multiple FEB/D modules is made possible by a connection to the Clock&trigger module through a ERNI SMC connector carrying LVDS signals at 400 Mbit/s. This interface also provides for a trigger system allowing to discard events records that are not part of a coincidence. Such events records are not transmitted to DAQ board.

A Gbit Ethernet communication mezzanine is also available for use with small systems. When using the Gbit Ethernet communication mezzanine the maximum data output rate to the computer is 15 M events/s.

The middle mezzanine (the red board) on figure 6 supplies bias voltages to the SiPMs. The de default mezzanine provides 16 positive bias voltages in the range 0-72 V, with a maximum current of 2.5mA per bias line. We can provide a version providing a maximum current of 8.75 mA per line. We also can provide a different bias voltage mezzanine with 64 bias voltage lines, same voltage range, 8 per FEM128. In this case the maximum current is 550mA per bias line. It is possible to connect an external power supply and in this way provide up to 50 mA per bias line.

A non-standard bias mezzanine, supplying a larger current, is also available.

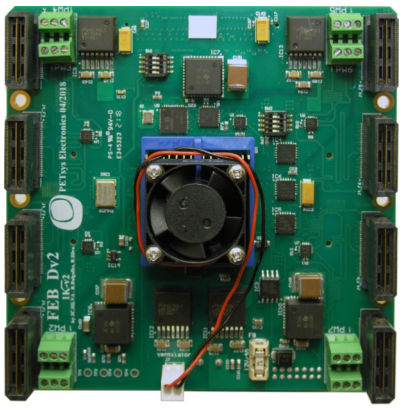

Figure 7.
Bottom side of the FEB/D-1k mother board showing the 8 connectors receiving the cables from the FEM128 modules.

Main features of the FEB/D-1k module:

- Reading up to 1’024 independent SiPM channels from 8 FEM128.
- Equipped with Kintex-7 FPGA.
- Comes with pre-installed firmware.
- Connects to up to eight Front-End Modules with 128 channels.
- Choice of two Data output DAQ mezzanines: SFP+ optical/copper, or Ethernet.
- Max output rate 6.6 Gbps, or 100 M events/s.
- Up to 32 FEB/D-1k modules can be Daisy chained and connected to a single DAQ board input.
- Receives clock and synchronization signals from the Clock&Trigger module.
- Clock frequency 200 MHz.
- External supply voltage: 12 Vdc, maximum 4 A.
- On board DC-DC converters supply power to the ASICs in the FEM boards.
- SiPM bias voltages produced in a mezzanine. The default mezzanine provides 16 lines, 5-100 V, positive, 3-9 mA per bias line.
- Can accept a veto signal from the Clock&Trigger module..

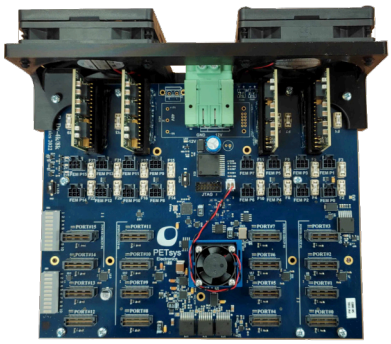

Figure 8
Top view of the FEB/D-8k mother board

The FEB/D-8k module.

Each FEB/D-8k module can control up to 16 of any of the front end modules, FEM128, FEM256 or FEM512 . The connection between the FEB/D-8k and the FEM uses the SAMTEC HQCD cable shown on figure 3. This cable can be up to 300 cm long

The FEB/D-8k is equipped with Kintex-7 and Spartan-7 FPGAs, and comes with the firmware installed. It receives event records from up to 128 PETsys TOFPET2 ASICs in the front-end modules (FEMs). It sends the event records as assembled in data frames through SFP+ high-speed links (either copper or optical cable) to the DAQ board in the data acquisition computer.

The FEB/D-8k provides clock synchronization signals to the ASICs and receives configuration signals from the DAQ board and distributes these to the ASICs. It receives the system clock (200 MHz), synchronization and trigger signals from the Clock&Trigger module.

Each FEB/D_8k board (Fig. 8 and 9) consists of a motherboard, measuring 208x166.3 mm^2, and three mezzanine boards on the bottom side of it. The green middle mezzanine (COMM-DAQm) provides the link to the DAQ board in the DAQ computer and the two red mezzanine boards provide bias voltages to the SiPM arrays. The default bias mezzanine board (BIAS-32)

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provides 32 positive bias voltages in the range 0~60 V, and an average current per bias line of 2 mA (5 mA option on request). Optionally we can provide the (BIAS-16P). This board provides 16-positive bias voltages up to 72 V and with an average current per bias line of 2.5 mA. Several FEB/D_8k boards can be daisy-chained and interfaced to a single DAQ board input. The maximum event rate of the high-speed link is 100 M events/s.

Synchronous readout of multiple FEB/D modules is made possible by a connection to the Clock&trigger module through a ERNI SMC connector carrying LVDS signals at 400 Mbit/s. This interface also provides for a trigger system allowing to discard events records that are not part of a coincidence. Such events are not transmitted to DAQ board.

The FEB/D_8k board needs to be supplied with 12 Vdc, maximum 25 A. The current depends on the type and number of FEM connected to it. Four DC-DC converters (visible on the top side of the mother board) and regulators provide power to the ASICs.

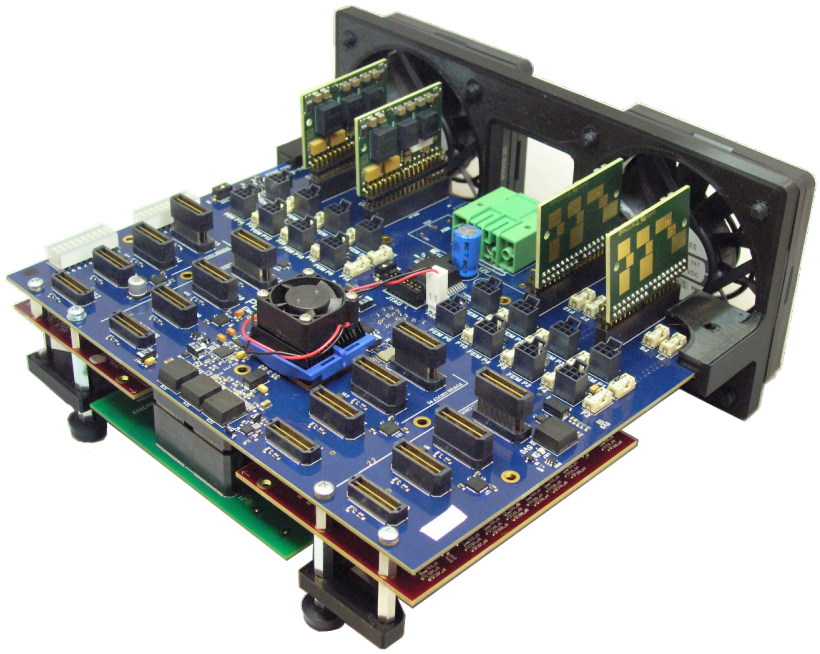

Figure 9. PETsys FEB/D-8k module.
On the top side of the mother board there are four 4 DC-DC converters providing power to the ASIC and 16 connectors for the FEM modules. Under the mother board there are two bias mezzanines and one communication mezzanine

Main features of the FEB/D-8k module:

- Reading up to 8'192 independent SiPM channels from 16 FEM modules.
- Equipped with Kintex-7 FPGA and Spartan-7 FPGAs.
- Comes with pre-installed firmware.
- Connects to up to 16 Front-End Modules ; FEM128, FEM256 or FEM512.
- Choice of two Data output DAQ mezzanines: SFP+ optical/copper, or Ethernet.
- Max output rate 6.6 Gbps, or 100 M events/s.
- Up to 32 FEB/D-8k modules can be Daisy chained and connected to a single DAQ board input.
- Receives clock and synchronization signals from the Clock&Trigger module.
- Clock frequency 200 MHz.
- External supply voltage: 12 Vdc, maximum 25 A.
- On board DC-DC converters supply power to the ASICs in the FEM boards.
- SiPM bias voltages produced by two mezzanine boards. The default mezzanine type provides 32 biasing lines, independently configurable to 0-60 V, and able to supply 2 mA per bias line on average.
- Can accept a veto signal from the Clock&Trigger module..

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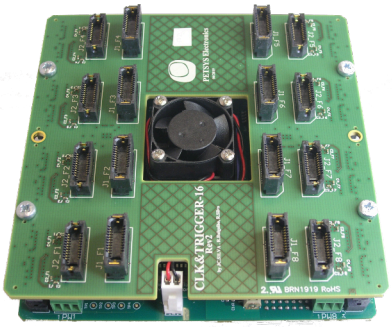

Figure 10: Clock&trigger module.
Bottom view showing the connectors for 16 Samtec ERCD cables providing clock an trigger signals to the FEB/D modules.

§ 4. The Clock&trigger module.

All FEB/D modules are connected to the Clock&trigger (Fig. 10) module using a flat coax cable Samtec ERCD-010-80.00-TBR-TBR-1-N. The Clock&trigger module provides clock signals and synchronization signals to the FED/D modules, and allows implementing a system wide coincidence filter. It collects coarse time information from all the FEB/D modules and tells the FEB/D modules which events are part of a coincidence.

The Clock&trigger module uses the same mother board as the FEB/D board. It has the same communication mezzanine and uses the same communication protocol as the FEB/D modules, and connects to the DAQ board in the same way. It can be daisy-chained with the FEB/D modules to connect to the DAQ module.

The Clock&trigger board supports up to 16 FEB/D and 4 trigger regions per FEB/D. A Clock&Trigger board for larger systems can be developed on request.

For synchronization with external systems, it can accept an external clock and synchronization signal or it can provide a clock and synchronization signal to an external system. It can also accept a veto signal which causes all events across all FEM to be discarded when it's active.

§ 5. The DAQ module.

The DAQ module (Fig, 11) plugs in the DAQ computer. It is equipped with a Kintex-7 FPGA. It collects data from the FEB/D boards, and transmits the data to the DAQ computer using a x4PC_express port.

The DAQ module has 3 SFP+ optical/copper connectors connecting to 3 chains the FEB/D boards transmitting data at 6.6 Gbps each.

The DAQ board receives and merges the data frames and transmits the assembled data frames to the computer. The maximum event record rate to the DAQ computer is 200 Mcps. This corresponds to a data rate of 13.3 Gbps. The DAQ module also sorts the events in the data frames by chronological order to facilitate processing by software.

Several FED/D modules can be daisy chained and send their output over the same optical link to the DAQ board. In this way the DAQ board, the Clock&Trigger module and the FEB/D modules together form a complete and scalable data acquisition system that can handle tens of thousands of SiPM channels.

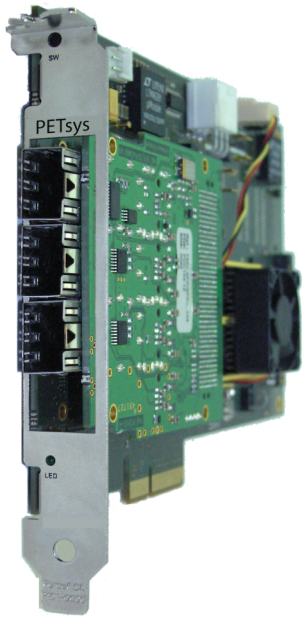

Figure 11: DAQ module.
The DAQ module plugs directly into the PCI express bus of the DAQ computer. The three SFP+ connectors on the front panel receive the 3 SFP+ copper links or optical links from the FEB/D chains.

Main features of the DAQ module.

- Single PCI express board providing data acquisition with TOF ASICs.
- Equipped with Kintex 7 FPGA.
- Compatible with FEM128, FEM256, FEB/D-1k FEB/D-8k, and Clock&Trigger modules.
- Equipped with 3 SFP+ optical/copper connectors receiving three otical links for sending and receiving data to/from three FEB/D module chains.
- Distributes configuration files for the ASICs.
- Configures the Clock&Trigger module.
- Maximum total input event rate: 100 M events/s for each of the input links.
- Maximum data output rate to the DAQ computer: 200 M events/s.
- Reads temperature sensors in the Front-End Modules.
- Reads internal counters in the TOFPET ASIC .
- Accepts an external veto signal and distributes it to the FEB/D boards via the Clock&Trigger module.

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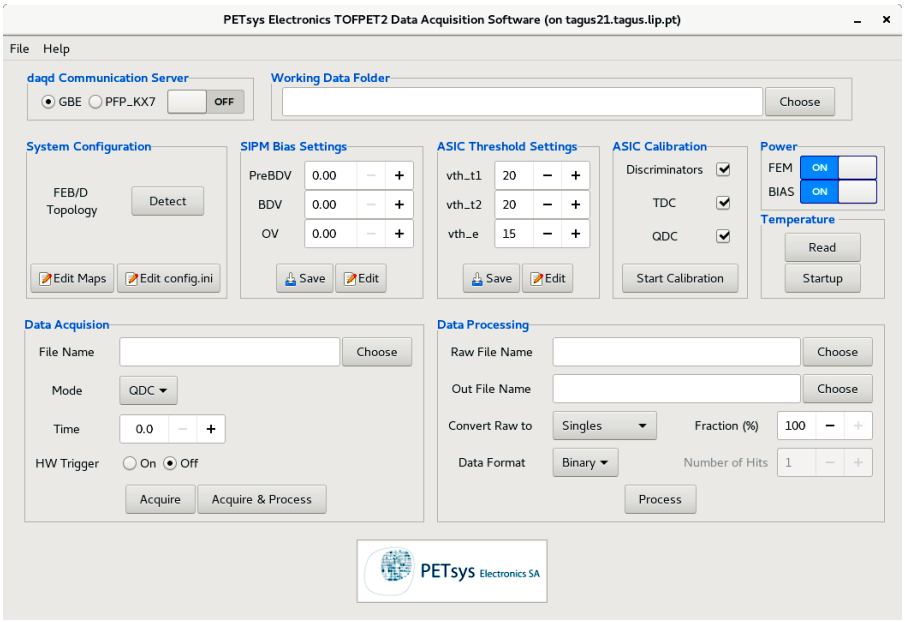

Fig. 12: Graphical user interface.
The data acquisition is controlled by an easy to use graphical user interface.

§ 6. DAQ firmware and software.

The PETsys readout system is provided with firmware and software. The data acquisition software runs under Linux (Red Hat Enterprise Linux 8, CentOS 8 Stream, or Ubuntu) and comes with an easy to use graphical user interface, see figure 12. The software is written in Python and C++, and is also provided as source code, allowing the advanced user to customize it under the MIT open source license.

The firmware implements a software centric approach, allowing direct and online access to PETsys TOFPET 2 ASIC configuration, to the bias voltage configuration, to the temperature sensor readout and to the uncalibrated (raw) TOFPET 2 ASIC data.

In order to reduce the data rate to the DAQ computer, the firmware in the FEB/D modules supports coincidence event selection. The coincidence event selection is based on coarse time stamps (1 clock period, 5 ns). The complete readout system can be divided in a configurable number of trigger regions, and events without a coincidence partner in a different trigger region are discarded and not transmitted to the DAQ computer. The smallest trigger region consists of two FEM128 connected to the same FEB/D-1k. Besides the optional rejection of events that are not part of a coincidence, no other manipulation is performed on the raw event data from the TOFPET 2 ASIC.

The coincidence filter searches for coincidences between events above a configurable energy threshold, belonging to allowed trigger region pairs. The time difference between coincidence events is configurable to 0, 1, 2 or 3 clock periods. When coincidences are found, the coincidence filter will forward any events within a window (3... 16 clock cycles) of the primary trigger events. The duration of the windows and the matching of the trigger regions is configurable.

The coincidence filter allows collecting of data for two types of random coincidence correction methods:

- Wide coincidence window: The coincidence window can beset to a value larger than2 clock cycles, allowing the collection of more random events; this is broadly equivalent to the delayed window method.
- Periodic single trigger: In addition to coincidences, the trigger can select all events in a window of 10, 20, 50 or100 clock periods every1025 clock periods. The1025 clock periodicity ensures that the data collected is de-correlated from the systems' 1024 clock frame period.

Synchronization with other systems.

It is often necessary to synchronize the clock on the PET readout with other clocks in the system. If the ratio of the clocks frequencies of the two sub systems is an integer, both can share a common clock and synchronization signal. The FEB/D board or the Clock&trigger module can accept an external signal and generate a event record with a time least count of 1.24 ns. Alternatively, one can use any ASIC input channel to generate time event records with a timing least count of 30 ps. Finally, the Clock&trigger module can send out LVDS timing signals synchronized to the ASIC clock at a configurable frequency.

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§ 7. Examples of readout solutions.

The readout was developed with the application in Time of flight PET in mind, but it can also be used in many other applications where one needs to read a large number of SiPM pixels. The Front-End Modules, the Front End type D module, the DAQ board and the Clock&Trigger module together allow building data acquisition systems adapted to the needs of most applications. Below we present 4 typical applications in PET.

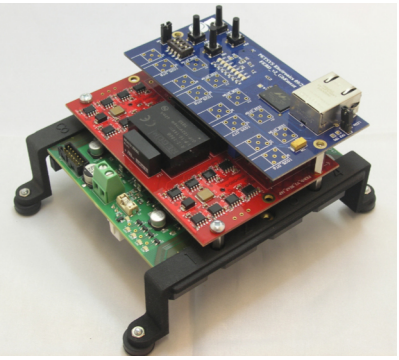


Figure 13. FEB/D-k for small systems.

Figure showing a FEB/D-1k module with Ethernet mezzanine. The FEB/D-1k module collects data from up-to eight FEM128, and sends the data to a computer using an Ethernet link at 1Gbit/s.

Readout solution for small systems.

If the application requires1'024 channels or less, and if the total data rate to the computer is below 15 M events/s after coincidence event selection, the readout will need one FEB/D-1k equipped with an Ethernet communication mezzanine (Fig. 13), and maximum eight FEM-128. The maximum number of events that can be sent to the DAQ computer in one interval of 1024 clock cycles (5120 ns) is limited to 1022.

For the purpose of coincidence event selection, the Front-End Modules connected to one FEB/D can be divided in maximum four trigger regions. A trigger region consists of either one or two FEM128.

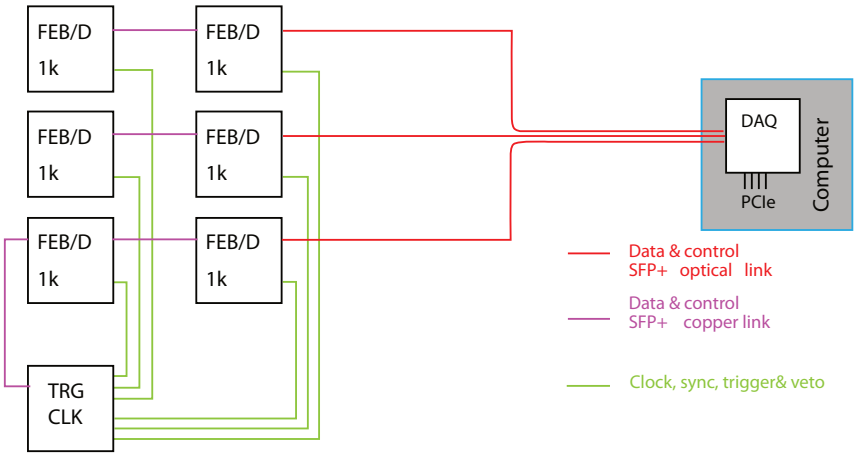
Readout solution for several 1'000 channels.

If the application requires reading more than 1'024 channels, or requires a larger event rate to the computer, the system needs a Clock&Trigger module and a DAQ module, see figures 10 and 11. Figure 14 shows system interconnect topology for a system with 6'144channels. It can be extended to more channels by daisy chaining more FEB/D- boards. One chain of FEB/D boards can have up to 32 boards. Each ASIC has 4 LVDS data output links, and the maximum data output rate from the ASIC to the FEB/D-1k is 500 kcps per ASIC channel.

In most cases the data rate from the DAQ board to the computer (200 M events/s) will be limiting the event rate per channel. The useful event rate will depend on the efficiency of the coincidence filter. The efficiency of the coincidence filter depends on the geometry of the PET scanner considered; it typically reduces the data rate to the computer by a factor 10. For example, in a PET system with 6'144 channels, the maximum single event data rate the system can handle is of the order of 500 kcps foreach channel. Also in this case the maximum number of events that can be sent to the computer in one interval of 1024 clock cycles (5120 ns) is limited to 1022.

Figure 14. System with 6'144 channels.

System interconnect topology for a readout with 6 FEB/D-1k modules. Each FEB/D-1k is connected to eight FEM128. In this example the communication between the master FEB/D module and the DAQ computer uses optical fibers, and the communication between the FEB/D modules in the FEB/D daisy chain uses SFP+ copper links.



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Readout solution for several 10’000 channels.

A new version of the readout solution with a front-end module reading 256 channels (FEM256) and a FEB/D_8k module is now available. It allows reading up to 65’536 channels. This readout is optimized for a lower per channel cost in applications such as Whole Body PET. In the FEM256 module only 2 data output lines per ASIC are used and the maximum event rate from the ASIC to the FEB/D is 300 kcps per channel.

Figure 4 shows the FEM256 board. It has 4 PETsys TOFPET ASICs and connects to the FEB/D boards using the same Samtec cable shown on figure 3. This FEM256 board connects to the FEB/S with the SiPM arrays with a flat flex cable as shown in Figure 5. The aluminum cooling bar in this figure is only to illustrate the cooling concept to be used in this case. The user can adapt the cooling to his particular scanner geometry. The FEB/D_8k module (Fig. 8, 9), connects to 16 FEM256. This readout solution uses the same Clock&Trigger module and the same DAQ board as the readout with FEM128 and FEB/D1k modules.

Figure 15 shows the system interconnect topology of a system reading 32’768 channels. The system has 8 FEB/D_8k, 128 FEM256, one DAQ board and one Clock&trigger module. The average event rate per channel will be limited by the data transfer rate to the computer. In this example the maximum event rate per channel will be 60 kcps if the coincidence trigger reduces the data rate by a factor 10. Using the same DAQ board and the same Clock&Trigger module the system can straightforwardly be extended to reading 65’636 channels. In combination with the new FEM/512 (under development), this allows reading up to 131’272 channels

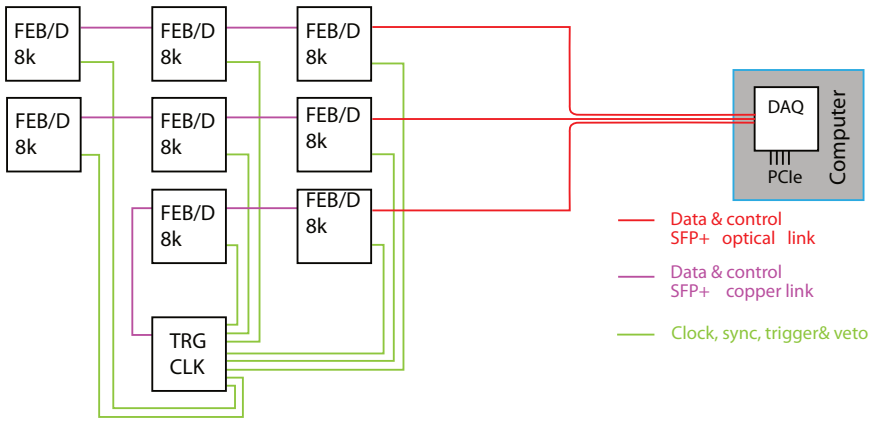

Figure 15. Interconnect topology for a system with 32’768 channels.

The system has 128 FEM256 boards connected to 8 FEB/D-8k.This solution can be extended to reading up to 65’488 channels

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Readout solution for reading more than 131’272 channels.

A total body PET scanner may requires reading several 100’000 SiPM pixels.

Figure 16 shows the interconnect topology for a system reading 196’608 electronic channels. This example has 24 FEB/D-8k modules, one Clock&trigger module and 2 DAQ modules. The system uses the FEM512 (not discussed in this document), and the same FEB/D-8k and DAQ module as described in this document. However, It requires a different Clock&trigger module supporting more than 16 FEB/D modules. It may require several DAQ modules to allow for a sufficient data rate to the computer. The two or more DAQ modules can either be plugged in the same computer of in different computers.

It is possible to reduce the number of electronic readout channels by using some multiplexing scheme, but such schemes usually degrade the coincidence time resolution.

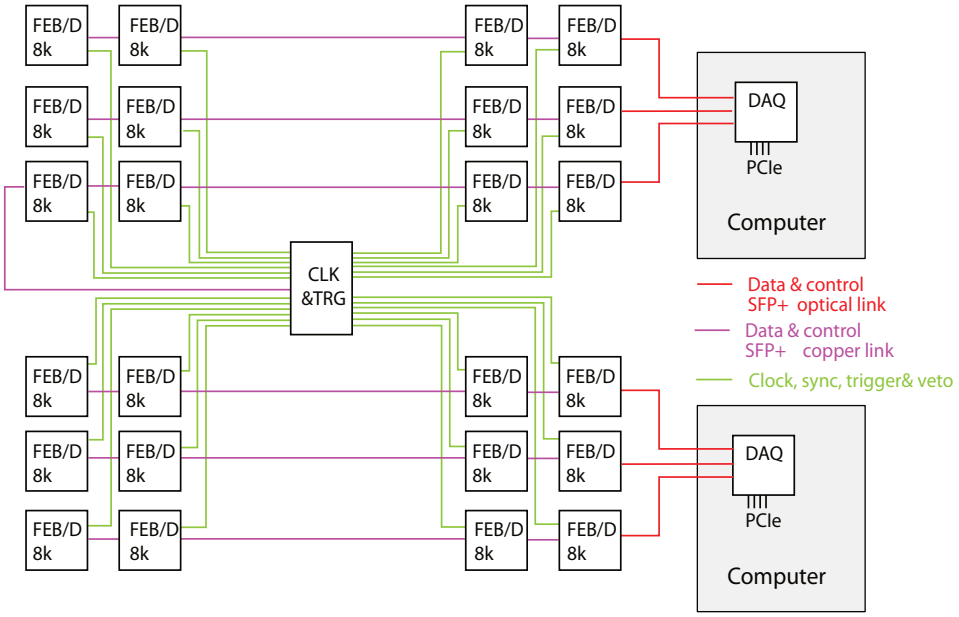

Figure 16. Readout for a system with 196’608 channels.

The systems has 2 DAQ boards and 6 chains with 4 FEB/D-8k modules each. Three chains of FEB/D-8k are connected to each DAQ board using one optical link.

On our web site www.petsyselectronics.com/documentation there is extensive technical documentation about our electronics

Contact “sales@petsyselectronics.com” for any question

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